ENGR-190: Introduction to Digital Logic Laboratory

Lab Procedures

Attendance
Attendance is mandatory. Each student must complete all labs in order to receive a passing grade. If you miss a lab without prior notification of the instructor, you will be required to make up the lab subject to up to a 50% penalty in grade. No penalty will be imposed if an arrangement is made with the instructor prior to the lab.

Lab Preparation
Most labs require the preparation of a pre-lab that may involve a significant amount of work. The pre-lab must be completed prior to arrival at the lab. The pre-lab work will be graded as you enter the lab and is part of your lab grade.

Reports
Lab reports are due at the end of each lab. Each report must be written neatly and must be organized in a way that is easy to read. Each report must include the following information as applicable:

The purpose of the lab report is to show that you understand the concepts and are able to execute the procedures and make the circuits work.

- Lab # & Date
- Student names (author first)
- Lab Title and Objective
- Each procedure described to show the process adequately
  - Each procedure a separate section
- Circuit diagrams/ codes
- Truth table for combinational logic
- Timing diagrams
- New concepts since last lab
- Analysis and conclusions, correct, and in clear language.

Circuit diagrams must include IC# and gate# as shown in the diagram above. All pins must be labeled. (Power and ground connections must be drawn for first three labs). A legend listing all ICs (e.g., U1 7400 Quad NAND) must be a part of each circuit diagram.
Note: Pin numbers and IC designations are required for any circuit that will be hand-wired on the logic trainer. Diagrams executed in Quartus and Cedar that are not tied to specific chips will not need pin numbers or IC designations. Verilog code will be organized according to standard practice demonstrated, and must be adequately documented.

Quartus projects, gates and Verilog must include documented output.
ENGR-190: Introduction to Digital Logic Laboratory
Laboratory #1: Logic Trainer & basic gates

Purpose
The purpose of your first lab is to become familiar with the features and devices on the Logic Trainer.
Learn how to document and wire a logic diagram.

Part 1: Lab process
a. The diagram to the right shows a Cedar simulation of the basic gates, not, or, xor, nand and nor. Open the provided file with Cedar and verify the operation of all the gates. Create a truth table for each, using the results from the Cedar simulation.

b. Delete the wire from the not gate (inverter) to the output LED by clicking on it then pressing Delete. Replace the wire on the inverter output and wire to the LED input (on the left).

c. Explore the options at the left of the Cedar screen to get a feel for building circuits in Cedar. Then click on the page 2 tab on the Cedar screen and implement the following circuit. Demonstrate its operation to the instructor.

d. Write a short paragraph describing your experience with this exercise. Did it work?

Part 2: Equipment familiarization
a. Logic trainer: Learn how to use the following features of the Logic Trainer: Power Switch, Power Supply terminals: +5 V (Vcc) & ground (do not use + 15 V and -15 V), Logic indicators, Data and switches, Clock: waveform and frequency selection, Breadboard connections: buses and tie points.
Learn the scheme of the connections on the board and locations of all controls and test signals and power sources.
Note containers with different sizes of wire. Learn how to place wires on the logic trainer (check that power is off first). Verify the connections against the logic diagram.

b. Test one gate each on the 7408 and 7432. (check the pin numbers for power, inputs & outputs for each gate.

Clean up At the end of the lab. Return the lab to its original condition.
Turn off power to all devices. Remove wires and components from Digital Trainer. Return
components to appropriate storage bins. Clean up the work bench.

Logic Trainer Practice

Follow the instructor’s remarks on the trainer. Make sure you understand, and that you know the location and purpose of the following:

Insert breadboard instructions here:

Test procedure:

A. On the Logic Trainer, Make the connections shown by your Instructor to install the chips on the proto-board. Test the operation of the chips. Just test one gate on each chip.

   Document that you’ve made a complete test of the gates.

   

   **TRUTH TABLE**

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B. Identify and document the pin numbers for the chips in this diagram.

   Build the circuit for \((Y = A \cdot B + A \cdot B)\) and test it.

   Show that your test is complete
## TRUTH TABLE

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Questions to answer:

1. What did you demonstrate that you haven’t done before?
2. What is a truth table?
3. How can we be sure we’ve tested all possible inputs?
4. What are the logic values and corresponding voltage ranges?
5. What can the LEDs on the trainer detect?
6. What levels are detected by the Logic Probe?